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Serial No. 09/170,336
Art Unit No. 2674

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of :	July 6, 2004
J. S. Beeteson, et al :	Group Art No.: 2674
Serial No. 09/170,336 :	Examiner: K. M. Nguyen
Filed: October 13, 1998 :	IBM Corporation by Anne Vachon Dougherty 3173 Cedar Road Yorktown Hts, NY 10598

Title: ACTIVE CORRECTION TECHNIQUE FOR A MAGNETIC MATRIX DISPLAY

Board of Patent Appeals and Interferences
Washington, D.C. 20231

APPEAL BRIEF (37 CFR 1.192)

Appellants hereby appeal to the Board of Patent Appeals and Interferences from the decision dated February 5, 2004 of the Examiner finally rejecting Claims 1-11 in the above application, and respectfully request that the Board of

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Patent Appeals and Interferences consider the arguments presented herein and reverse the Examiner's rejection.

I. REAL PARTY IN INTEREST

The appeal is made on behalf of Applicants who are real parties in interest with respect to the subject patent application.

II. RELATED APPEALS AND INTERFERENCES

There are no pending related appeals or interferences with respect to the subject patent application.

III. STATUS OF CLAIMS

There are eleven (11) claims pending in the subject patent application, numbered 1-11. No claims stand allowed. All of Claims 1-11 stand rejected.

A complete copy of the claims involved in the appeal is attached hereto.

IV. STATUS OF AMENDMENTS

The status of the prosecution of the application is as follows:

May 9, 2000	-	Office Action.
September 8, 2000	-	Amendment
November 2, 2000	-	Office Action
January 30, 2001	-	Amendment
March 7, 2001	-	Office Action
July 9, 2001	-	Amendment
September 25, 2001	-	Final Office Action
February 25, 2002	-	CPA and Amendment
April 24, 2002	-	Office Action
July 24, 2002	-	Amendment
October 15, 2002	-	Final Office Action
March 17, 2003	-	Notice of Appeal
May 15, 2003	-	Appeal Brief filed
September 10, 2003	-	Withdrawal of Final Office Action and issuance of new Office Action citing new art
December 10, 2003	-	Amendment
February 5, 2004	-	Final Office Action
May 4, 2004	-	Notice of Appeal

V. SUMMARY OF INVENTION

The subject invention is a matrix-addressed display device having a cathode means; a grid electrode means, wherein the grid electrode means comprises a first plurality of parallel row conductors and a second plurality of parallel column conductors arranged orthogonally to the row conductors; and, a means for providing cut-off correction information and gain correction information to one of the first plurality or the second plurality of conductors.

VI. STATEMENT OF ISSUES OF APPEAL

There following issues are on appeal:

(1) whether the Examiner correctly stated the claimed invention when rejecting the sole independent claim, Claim 1;

(2) whether the display device as recited in Claims 1-5 is patentable over U. S. Patent 6,121,942 of Sanou, et al (hereinafter "Sanou");

(3) whether the display device as claimed in Claim 6 is patentable over the combined teachings of Sanou in view of U. S. Patent 5,818,403 of Nakamura, et al (hereinafter "Nakamura");

(4) whether the display device as claimed in Claim 7 is patentable over the combined teachings of Sanou in view of the Nakamura and further in view of the Applicant Admitted Prior Art (hereinafter "AAPA);

(5) whether the display device as claimed in Claim 8 is patentable over the combined teachings of Sanou, in view of Nakamura and further in view of U. S. Patent 5,594,463 of Sakamoto (hereinafter "Sakamoto"); and

(6) whether the display device as claimed in Claims 9-11 is patentable over the combined teachings of

Sanou in view of U. S. Patent 5,262,698 of Dunham (hereinafter "Dunham").

VII. GROUPING OF CLAIMS

The Claims can be considered in the following groups for purposes of this appeal:

(I) Group I: Claims 1-2, wherein the matrix addressed display device is detailed to include the cathode means, grid electrode means comprising a first plurality of row conductors and a second plurality of column conductors, and means for providing cut-off correction information (Claim 1) and gain correction information (Claim 2) to one of the first plurality or the second plurality of conductors;

(II) Group II: Claims 3-4, the device of Claim 1 further comprising memory (Claim 3) and screen (Claim 4);

(III) Group III; Claims 5-7, the device as recited in Claim 1 and further comprising applying correction information to only the first plurality of conductors (Claim 5) and wherein correction information is chosen to compensate for variations during warm up (Claims 6-7);

(IV) Group IV; Claims 8-11, the device as recited in Claim 1 wherein temperature and location affect the values of the cut-off and gain correction information to be supplied.

VIII. ARGUMENTS

ARGUMENT (1)

With regard to issue (1), whether the Examiner correctly stated, and correctly examined, the claimed invention when rejecting the sole independent claim, Claim 1, Appellants refer the Board's attention to the language of Claim 1 and to the Examiner's statements in the Final Office Action from which Appellants are appealing. The language of Claim 1 recites "[a] matrix addressed display device comprising: a cathode means; grid electrode means comprising a first plurality of parallel row conductors and a second plurality of parallel column conductors arranged orthogonally to the row conductors; characterised in that the display device further comprises: means for providing cut-off correction information to ***one of said first or said***

second plurality of parallel conductors" (emphasis added). In contrast, the Examiner has stated, on page 2, paragraph 2, line 7 and at page 6, paragraph 9, lines 4-6, "the field emission display FED which includes providing cut-off correction information ***...to one of a row plurality of parallel conductors*** Dx1 to Dxm".

Appellants respectfully assert that the Examiner has restated the claim language in order to make the cited references applicable. Appellants are not claiming a means for providing cut-off correction information to one conductor or device in a row of first of parallel conductors. Appellants are claiming a means for providing cut-off correction information to one of said first or said second plurality of parallel conductors (i.e., to the first plurality or to the second plurality). Appellants respectfully argue that the Examiner has not correctly stated the claim language and has not, as a result, correctly examined the invention as claimed.

ARGUMENT (2)

As to issue (2), whether the display device as recited in Claim 1 is patentable over U. S. Patent 6,121,942 of

Sanou, et al (hereinafter "Sanou"); Appellants submit the following arguments.

The subject application teaches and claims a matrix addressed display device comprising a cathode means, grid electrode means comprising a first plurality of parallel row conductors and a second plurality of parallel column conductors arranged orthogonally to the row conductors; and means for providing cut-off correction information to a one of said first or said second plurality of parallel conductors, as is specifically recited in independent Claim 1, and all of the remaining claims which depend therefrom.

Under the present invention, cut-off correction information and, optionally, gain correction information as well, is provided to one of a first plurality of parallel conductors (e.g., rows) or a second plurality of parallel conductors (e.g., columns) along with the drive voltage information which is being provided to those conductors based on the image display desired. As set forth in the teachings found from lines 11-27 on page 12 of the Specification, "[w]hen a particular column driver is not selected, the column grid conductor...is driven to a non-selected voltage, that is a voltage below cut-off" and

"when a column driver 502 is selected...[it is] driven to a cut-off voltage" and "[t]he level of drive to the...conductors is determined by the pixel data...and the correction data 516 supplied from...memory. The correction data 516 consists of cut-off and gain corrections."

As further taught in the Specification at page 6, lines 19-23, "[t]he provision of cut-off correction information allows the cut-off of individual rows or columns to be adjusted, so as to reduce luminance variations." The Specification goes on to teach that all of the plurality of conductors can receive the same correction information, as in the "warm up" correction situation taught at page 11, lines 16-18, or each of the plurality of conductors can receive a specific correction value based on its position in the array, as taught in the luminance variation situation taught at page 17, lines 20-25. In either case, ***all*** of the conductors in a plurality of conductors are receiving correction information along with the drive voltage information. Accordingly, what is taught and claimed is an device whereby the image information (e.g., cut-off voltage or a voltage below cut-off), and correction information is being supplied to all of a plurality of conductors.

Sanou teaches a display device comprising an array of electron-emitting devices which are aligned to fluorescent stripes. Upon application of a voltage to the electron-emitting devices, and application of a potential to the fluorescent layer above the array, electrons are directed to the fluorescent layer to cause it to fluoresce. Since misalignment of the electron-emitting devices and the fluorescent stripes results during manufacturing, the Sanou system provides a way to compensate for positional deviation in order to obtain the best display. Sanou describes the three misalignment problems and the solutions. For Y direction misalignment, as in Fig. 21, no adjustment is needed. For X direction misalignment, Sanou determines the needed correction voltage and applies it to the entire fluorescent stripe, as illustrated in Fig. 22 and detailed in the cited teachings from Col. 29. For skew, which involves both X and Y misalignment, correction must be provided for device separately, since the positional deviation varies from one row of devices to the next. For each device, the amount of needed correction is calculated one time and the correction voltage is stored in memory. Each time that device is used, its corresponding correction

voltage is read out of storage and applied along with the original voltage (determined with a perfectly aligned device in mind).

The cited teachings of Sanou at Col. 29, lines 1-23 teach changing the voltage 87 on the fluorescent material in order to compensate for the misalignment between the material and the corresponding electron-emitting devices. As shown in cited Fig. 24, the voltage from 87, Va, is provided to the fluorescent layer (see: Col. 28, lines 61-64). Appellants respectfully assert that the cited passages of Sanou do not anticipate the invention as claimed. Applying potential to a fluorescent stripe is not the same as, nor suggestive of, a device wherein ***all*** of the conductors in a plurality of conductors are receiving correction information along with the drive voltage information.

It is first to be noted that correcting the voltage based on misalignment is not the same as nor suggestive of providing cut off correction or gain correction. As pointed out to the Examiner in the earlier prosecution of this application, "cut off correction" and "gain correction" are terms of the art and cannot be anticipated by other

correction values that are not specifically gain or cut off correction. Further, the Sanou system recalculates the operating voltage for the device and effectively re-sets the operating voltage. Such is not the same as or suggestive of providing cut off or gain correction. Furthermore, Sanou expressly teaches in the cited passage from Col. 29 that the voltage on the fluorescent material is altered. Such teachings neither anticipate nor obviate the claim language wherein cut off correction information is provided to one of the first set of parallel conductors or the second set of parallel conductors. The cited Sanou teachings do no alter the voltage on the "Dy1-Dym" or the "Dx1-Dxn" electron-emitting devices. Rather, Sanou alters the voltage on the fluorescent material which is located opposite to the electron-emitting devices.

Under 35 USC 102, for a patent to anticipate claim language, that patent must teach each and every claim feature. Since the cited teachings of the Sanou patent do not teach means for providing cut off correction information to one of said first or said second plurality of parallel conductors, it cannot be maintained that Sanou anticipates the language of Claim 1. It is also well established that a

reference that does not anticipate the language of an independent claim cannot be said to anticipate the language of dependent claims which depend therefrom and add limitations thereto. Accordingly, Appellants assert that the Sanou patent does not anticipate the language of Claims 2-5.

Claim 2 additionally recites means for providing gain correction information to one of the first or said second plurality of parallel conductors. There is nothing in the Sanou patent which either teaches or suggests providing gain correction information to a first or a second plurality of parallel conductors. As discussed above, Sanou either applies a potential across a fluorescent stripe or applies a pre-determined stored additional voltage to a single device. Clearly the language of Claim 2 is not anticipated by Sanou.

With regard to Claim 3, which recites the display device as claimed in claim 2 further comprising a non-volatile memory for storing a plurality of values for the cut-off and gain correction information, Appellants aver that Sanou does not teach the use of cut-off or gain correction information. Sanou stores an additional voltage

for a device to compensate for misalignment; however, such is not what is being expressly claimed.

Claim 4 recites the display device as claimed in claim 3, further comprising a screen for receiving electron beams modulated by the grid electrode means, the screen having a phosphor coating facing the grid electrode means, the phosphor coating comprising a plurality of pixels each corresponding to a different row or column. Appellants contend that while Sanou has fluorescent stripes, such is not the same as the invention of Claim 4 which includes all of the limitations of Claims 1-3 plus the phosphor coated screen.

With regard to Claim 5, which recites the display device as claimed in claim 3, wherein the cut-off and gain correction information is provided to the first plurality of parallel conductors, the gain and cut-off correction information being applied to all of the first plurality of parallel conductors, Appellants reiterate that Sanou is not teaching or suggesting the use of gain or cut-off correction information, let alone the application of same to an entire row or an entire column of parallel conductors.

Based on the foregoing, Appellants maintain that the Sanou patent does not anticipate the invention as set forth in Claims 1-5.

ARGUMENT (3)

As to issue (3), whether the display device as claimed in Claim 6 is patentable over the combined teachings of Sanou in view of U. S. Patent 5,818,403 of Nakamura, et al (hereinafter "Nakamura"); Appellants submit the following arguments. Appellants rely on the arguments presented above in "ARGUMENT (2)" with regard to the applicability of Sanou.

The Nakamura patent teaches a driving method for an electron beam generation system with image forming apparatus associated therewith. The Nakamura system includes rows of parallel electron-emitting device lines arranged in an XY matrix with columns of parallel modulation electrodes. The Nakamura method comprises alternately applying information signals to odd-numbered rows of electrodes in a parallel array of rows while applying cut-off information signals to the even-numbered electrodes in the parallel array; and, then, reversing the process to apply information signals to even-numbered rows of electrodes while applying cut-off

information signals to the odd-numbered electrodes (see: e.g., Col. 5, line 65 through Col. 6, line 5). Nakamura alternates application of its signals in order to reduce the negative (e.g., capacitance) effects experienced between neighboring modulation electrodes (see: e.g., Col. 5, line 46-50).

It is first to be noted that the Nakamura meaning of the term "cut-off" is actually not consistent with the meaning of "cut-off" in the present application. The Nakamura patent uses the term "cut-off" to mean non-information signals to be applied to non-selected rows (e.g., the even rows) to suppress conduction therein; while the present invention uses the term "cut-off" to mean the voltage applied to all selected conductors, in accordance with the formula detailed on pages 5-6 of the Specification for reducing luminance variations (see: page 6, lines 20-23). Further, what Nakamura teaches is the application of cut-off voltage alone and not the provision of additional signal correction information to the conductors. Finally, it is quite clear in Nakamura that the cut-off signals are being applied to only half of the electrodes in a plurality of electrodes (the driving method detailed at Col. 5, lines

41-46), whereas the present invention is teaching and claiming the application of correction information to all of the first plurality of row conductors or to all of the second plurality of column conductors.

Since the Nakamura method is directed to alternately applying signals to the odd and even numbered columns in one plurality of conductors, Appellants respectfully argue that one having skill in the art would not be motivated by the Nakamura teachings to modify the Sanou system, which teaches either applying a pre-determined signal to a single device or applying a potential to an entire stripe. Since Nakamura applies a signal to alternate columns, one would not look to it to modify Sanou and, even if one did modify it, would not arrive at a device wherein correction information is applied to all of a plurality of row conductors or all of a plurality of column conductors. Appellants believe that Nakamura clearly teaches away from such combination.

Appellants further note that to suggest that the current be applied to all rows or columns would render the Nakamura teachings unworkable, since applying the signals to all adjacent rows would be inconsistent with the Nakamura teaching of alternate application of voltage to reduce

negative effects. Clearly the Nakamura reference does not include any suggestion of such application of information to all rows or all columns. Moreover, since to modify the Nakamura teachings to apply the information to all rows or all columns would make it unworkable for its intended purpose, such could not be considered obvious. It is well established under U.S. Patent Law that modification of teachings cannot be considered obvious to one having skill in the relevant art if such modification would render the teachings unworkable for their intended purpose. Clearly, therefore, it cannot be maintained that the teachings of the Nakamura reference would logically be modified or used to modify Sanou, as further discussed below, and it cannot be maintained that any such modification would obviate the invention as claimed.

The Examiner has cited Nakamura for teaching cathode type devices, and that, as stated by the Examiner, "cold cathode type display devices are preferred". Claim 6 expressly recites that cut-off and gain correction information is chosen so as to compensate for variations in cut-off and gain occurring during warm up, which necessarily would be the type of variation encountered in hot cathode

devices. The Examiner states that "it would have been obvious to a person of ordinary skill in the art at the time of the invention to substitute the hot cathode being affected by temperature distribution taught by Nakamura et al for Sanou et al's cold cathode because this would provide a compensate image data occurring during warm up to obtain an image with high fineness, high sharpness, and high contrast *(sic)*" (see page 3, paragraph 3 of the Final Office Action). Appellants contend that the Examiner has not clearly articulated the grounds for rejection and Appellants find that they are unable to understand the reasoning behind the Examiner's statements. Further, Appellants believe that no motivation exists in the prior art to modify of combine the references (C. R. Bard, Inc. v. M3 Systems, Inc., 157 F. 3rd 1340, 48 USPQ 2d, 1225 (Fed. Cir. 1998)). Moreover, Appellants contend that it would not be obvious to modify Sanou with Nakamura, and, that any such modification would not render the language of Claim 6 obvious.

One would not look to Nakamura to modify Sanou since Nakamura expressly teaches applying signals to alternate rows and/or alternate columns of conductors. Sanou seeks to correct for misalignment by either applying a pre-determined

voltage to a single device or applying a potential across a particular misaligned fluorescent stripe. Clearly it would not be logical to apply the pre-determined voltage to alternate rows of devices, since all would not be similarly misaligned. Further, it would not be logical to modify Sanou to apply potential to alternate fluorescent stripes since, again, all stripes would not be similarly misaligned. Appellants maintain that one skilled in the art would not look to Nakamura to modify Sanou.

Even if one were to look to Nakamura for the sole teachings of hot cathode devices, although the Examiner has indicated that such is less desirable, Appellants respectfully assert that the inclusion of hot cathode devices to Sanou would still not obviate the language of Claim 6. Sanou modified by Nakamura would have different devices but would still apply a pre-determined stored voltage value to a single hot cathode device or apply a potential to a single fluorescent stripe. The modified Sanou would not, however, obviate the device including means for providing cut-off correction information to one of said first or said second plurality of parallel conductors to

compensate for variations in cut-off and gain occurring during warm up.

Accordingly, Appellants aver that Claim 6 is patentable over the combination of Sanou in view of Nakamura.

ARGUMENT (4)

As to issue (4), whether the display device as claimed in Claim 7 is patentable over the combined teachings of Sanou in view of the Nakamura and further in view of the Applicant Admitted Prior Art (hereinafter "AAPA"), Appellants submit the following arguments. Appellants rely on the arguments presented above in "ARGUMENT (2)" and "ARGUMENT (3)" with regard to the applicability of Sanou alone and in combination with Nakamura.

Claim 7 depends from Claim 6 and additionally recites the anode means and means for providing purity correction information anode means disposed between said grid electrode means, the anode means comprising a plurality of anodes extending parallel to the column conductors, the anode means comprising pairs of anodes each corresponding to a different column conductor, each pair comprising first and second anodes respectively extending along opposite sides of the

corresponding column conductor, the first anodes being interconnected and the second anodes being interconnected, and means for providing purity correction information across the first and second anodes so as to compensate for variations in purity occurring during warm up.

The Applicants' Admitted Prior Art, AAPA, from the Specification at page 1, lines 16-21 is a magnetic matrix display. The AAPA does detail anode means disposed between said grid electrode means, with the anode means comprising a plurality of anodes extending parallel to the column conductors, the anode means comprising pairs of anodes each corresponding to a different column conductor, each pair comprising first and second anodes respectively extending along opposite sides of the corresponding column conductor, the first anodes being interconnected and the second anodes being interconnected (see, page 1) but does not teach or suggest the means for providing purity correction information as claimed.

Appellants cannot agree with the Examiner's characterization of the AAPA found on page 4, paragraph 4 of the Office Action due to the confusing nature of the rejection. The Examiner concludes that "it would have been

obvious to a person of ordinary skill in the art at the time of the invention to substitute the anodes of each pair extend along opposite sides of the corresponding column of pixel wells 70. Each pixel well 70 is situated at the intersection of a different combination of a grid conductor and a column grid conductor taught by AAPA for Sanou et al's anodes because this would operate the electrons being released from the cathode and attracted towards the anode to hit the phosphor surface *(sic)*". Appellants again assert that the Examiner has not clearly articulated the grounds for rejection. Moreover, the Examiner has provided no evidence of motivation, such as a suggestion, in the prior art for the modification. Appellants adamantly assert that the AAPA provides no such motivation, and cannot find any motivation in the Sanou reference for such modification. Even if one were motivated to modify Sanou with the AAPA, the combination would still not teach or suggest the claim features of means for providing cut-off correction information to one of said first or said second plurality of parallel conductors, means for providing gain correction information to one of said first or said second plurality of parallel conductors (Claim 2), non-volatile memory for

storing a plurality of values for cut-off and gain correction information (Claim 3), wherein cut-off and gain correction information are chosen to compensate for variations during warm-up (Claim 6), as well as means for providing purity correction information across the first and second anodes so as to compensate for variations in purity occurring during warm up. Appellants do not believe that the Examiner has made a *prima facie* case of obviousness since not all of the claim features have been addressed adequately and motivation does not exist to combine the references (In re Wilson, 424 F. 2nd 1382, 165 USPQ 494 (CCPA 1970) and C. R. Bard, Inc. v. M3 Systems, Inc., 157 F. 3rd 1340, 48 USPQ 2d, 1225 (Fed. Cir. 1998)).

ARGUMENT (5)

As to issue (5) whether the display device as claimed in Claim 8 is patentable over the combined teachings of Sanou, in view of Nakamura and further in view of U.S. Patent 5,594,463 of Sakamoto (hereinafter "Sakamoto"), Appellants submit the following argument.

Claim 8, which depends from Claim 6, additionally recites temperature sensing means for determining which of said plurality of values of stored cut-off and gain correction information is supplied to one of said first or said second plurality of parallel conductors. Appellants first note that Claim 8 includes all of the limitations of Claims 1, 2, 3, and 6 and Appellants rely on the arguments set forth above in defense of that language.

In further rejecting Claim 8, the Examiner has cited the Sakamoto patent. Sakamoto teaches detecting a voltage drop and then providing a permanent voltage change to compensate for the voltage drop. The Sakamoto patent provides a temperature sensor in one embodiment (Col. 8, lines 1-9) wherein the temperature of the display panel is sensed and wherein the drive current value is decreased if the temperature exceeds a threshold and the voltage drop is corrected based on the temperature when the temperature does not exceed a threshold. Sakamoto does not provide the teachings which are missing from the combination of Sanou and Nakamura, including means for providing cut-off correction information to one of said first or said second plurality of parallel conductors, means for providing gain

correction information to one of said first or said second plurality of parallel conductors (Claim 2), non-volatile memory for storing a plurality of values for cut-off and gain correction information (Claim 3), wherein cut-off and gain correction information are chosen to compensate for variations during warm-up (Claim 6). Even if one were to modify Sanou in view of Nakamura with Sakamoto, one would arrive at a Sanou apparatus having a Sakamoto temperature sensor with hot cathode devices, wherein a pre-determined stored voltage value would be applied to a single hot cathode device or a potential would be applied to a single fluorescent stripe based on sensed temperature. The combination would not obviate the invention as claimed.

ARGUMENT (6)

As to issue (6), whether the display device as claimed in Claims 9-11 is patentable over the combined teachings of Sanou in view of U. S. Patent 5,262,698 of Dunham (hereinafter "Dunham"), Appellants note that Claims 9-11 all include the limitations of Claims 1-3. Accordingly, Appellants rely on the arguments set forth above in "ARGUMENT (2)" and "ARGUMENT (3)" and will not reiterate the

same arguments. In rejecting Claims 9-11, the Examiner has additionally cited the Dunham patent.

With regard to Claims 9-11, all of which recite the cut-off and/or correction voltages varying according to physical location, Appellants respectfully assert that Dunham does not provide the teachings which are missing from Sanou. Dunham teaches applying varying voltage levels at an emitting means at the intersection of two conductors. Dunham does not teach or suggest means for providing cut off correction information to one of a first or a second plurality of parallel conductors. In fact, Dunham's teachings regarding selectively applying varying voltage would not logically be applied to the cited Sanou teachings wherein Sanou seeks to alter the voltage on an entire layer of fluorescent material in order to compensate for the positional deviation of the entire fluorescent stripe relative to multiple devices, and not just for one device. With regard to the non-cited Sanou embodiment wherein voltage is applied to a single device, Sanou expressly stored one pre-determined value for voltage to be applied to that single device in order to compensate for positional deviation. It would not be logical to modify Sanou to

selectively apply varying voltages to a single device, since only one voltage adequately compensates for the deviation. One would not, therefore, be motivated to modify Sanou with Dunham since applying voltages other than the one pre-determined voltage would render Sanou unworkable for its intended purpose. Accordingly, Appellants believe that the two references would not logically be combined; and, that the combination would not result in the invention as claimed in Claims 9-11.

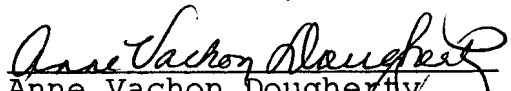
CONCLUSION

Appellants respectfully assert that the Examiner has erred in stating Claim 1, and in rejecting Claims 1-5 as anticipated by Sanou; Claim 6 as unpatentable over Sanou in view of Nakamura, Claim 7 as unpatentable over Sanou in view of Nakamura and further in view of AAPA, Claim 8 as unpatentable over Sanou in view of Nakamura and further in view of Sakamoto, and Claims 9-11 as unpatentable over Sanou in view of Dunham. Appellants believe that the Examiner has selectively reworded the claim language to fit the teachings of the references, that the references do not provide the

teachings or motivations which the Examiner has suggested, and that the combinations of teachings do not obviate the claims.

In light of the foregoing arguments, Appellants request that the decision of the Examiner, rejecting all of the pending claims, be overturned by the Board and that the claims be passed to issuance.

Respectfully submitted,
J. S. Beeteson, et al

By: 
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APPENDIX OF CLAIMS

1. A matrix addressed display device comprising:

a cathode means;

grid electrode means comprising a first plurality of parallel row conductors and a second plurality of parallel column conductors arranged orthogonally to the row conductors;

characterised in that the display device further comprises:

means for providing cut-off correction information to one of said first or said second plurality of parallel conductors.

2. A display device as claimed in claim 1 further comprising means for providing gain correction information to one of said first or said second plurality of parallel conductors.

3. A display device as claimed in claim 2 further comprising a non-volatile memory for storing a plurality of values for said cut-off and gain correction information.

4. A display device as claimed in claim 3, further comprising a screen for receiving electron beams modulated by said grid electrode means, the screen having a phosphor coating facing the grid electrode means, the phosphor coating comprising a plurality of pixels each corresponding to a different row or column.

5. A display device as claimed in claim 3, wherein said cut-off and gain correction information is provided to said first plurality of parallel conductors, said gain and cut-off correction information being applied to all of said first plurality of parallel conductors.

6. A display device as claimed in claim 3, wherein said cut-off and gain correction information is chosen so as to compensate for variations in cut-off and gain occurring during warm up.

7. A display device as claimed in claim 6, further comprising:

anode means disposed between said grid electrode means and said screen for accelerating electrons towards the screen, the anode means comprising a plurality of anodes extending parallel to the column conductors, the anode means comprising pairs of anodes each corresponding to a different column conductor, each pair comprising first and second anodes respectively extending along opposite sides of the corresponding column conductor, the first anodes being interconnected and the second anodes being interconnected; and

means for providing purity correction information across the first and second anodes so as to compensate for variations in purity occurring during warm up.

8. A display device as claimed in claim 6, further comprising temperature sensing means for determining which of said plurality of values of stored cut-off and gain correction information is supplied to a one of said first or said second plurality of parallel conductors.

9. A display device as claimed in claim 3, wherein said cut-off correction information is provided to said second plurality of parallel conductors, said cut-off correction information varying according to the physical location of each of said second plurality of parallel conductors.

10. A display device as claimed in claim 3, wherein said gain correction information is provided to said second plurality of parallel conductors, said gain correction information varying according to the physical location of each of said second plurality of parallel conductors.

11. A display device as claimed in claim 3, wherein said cut-off and gain correction information is provided to said first plurality of parallel conductors, said cut-off and gain correction information varying according to the physical location of each of said first plurality of parallel conductors and according to which of said second plurality of parallel conductors is selected.